

ABSTRACT OF THE DISCLOSURE

The present invention comprises a first MOS transistor whose gate and drain are connected with a first node, a second MOS transistor whose gate and drain are connected with the first node and a third node, respectively, a first resistive element which is connected between the first node and a second node, a second resistive element which is connected between the second node and a ground voltage terminal, a first NOT circuit whose input terminal is connected with the second node, whose output terminal is a fourth node, and which is connected between the third node and the ground voltage terminal, and a second NOT circuit whose input terminal is connected with the fourth node and whose output terminal is a fifth node. Consequently, the present invention can detect voltage in a stable condition with low power consumption.